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CERTIFICATE

I, Tadashi UEDA, residing at 1994-152, Hazama-machi, Hachioji-shi Tokyo 193-0941 Japan, hereby certify that I am the translator of the attached document, namely a Certified Copy of Japanese Patent Application No. 2003-019131 and certify that the following is a true translation to the best of my knowledge and belief.

Tadashi Ueda — January 10, 2006

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[Name of Document] Specification 1

[Name of Document] Drawings 1

[Name of Document] Abstract 1

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[Name of Document] SPECIFICATION

[Title of the Invention] THIN FILM TRANSISTOR TYPE DISPLAY DEVICE, METHOD OF MANUFACTURING THIN FILM ELEMENT, THIN FILM TRANSISTOR CIRCUIT BOARD, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC APPARATUS

[Claims]

[Claim 1] A thin film transistor type display device in which thin film transistors are formed on a first substrate, wiring lines are formed on a second substrate, and an element chip including one or more the thin film transistors is peeled off from the first substrate and transferred to the second substrate,

wherein holographic exposure is used in the patterning process of the thin film transistors.

[Claim 2] A thin film transistor type display device in which thin film transistors are formed on a first substrate, wiring lines are formed on a second substrate, and an element chip including one or more the thin film transistor is peeled off from the first substrate and transferred to the second substrate,

wherein a tracking focus system is used in the patterning process of the thin film transistors.

[Claim 3] The thin film transistor type display device according to Claim 1 or 2,

wherein a design rule of 1.0 μm or less is used in the

patterning process of the thin film transistors.

[Claim 4] The thin film transistor type display device according to Claim 1 or 2,

wherein only a polycrystalline silicon layer and a first metal layer are used as the wiring lines of the element chip.

[Claim 5] A method of manufacturing thin film elements including a step of transferring functional elements formed on a first substrate to a second substrate, the method comprising the steps of:

forming the functional elements in a predetermined shape on the first substrate via a peeling layer which causes peeling by the application of a predetermined amount of energy, and

transferring at least one of the functional elements to the second substrate by applying the energy to relevant portions of the peeling layer corresponding to the regions of the functional elements to cause peeling,

wherein holographic exposure is used to pattern the functional elements in the step of forming the functional elements in a predetermined shape..

[Claim 6] The method of manufacturing thin film elements according to Claim 5,

wherein the functional elements are thin film transistors.

[Claim 7] A thin film transistor circuit board comprising thin film transistors manufactured by a method of manufacturing the thin film elements according to Claim 6.

[Claim 8] An electro-optical device comprising a thin film transistor circuit board according to Claim 7.

[Claim 9] An electronic apparatus comprising an electro-optical device according to Claim 8.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to a thin film transistor type display device, and more specifically, it relates to a thin film transistor type display device in which thin film transistors are formed on a first substrate, wiring lines are formed on a second substrate, and an element chip including one or more thin film transistors is peeled off from the first substrate and transferred to the second substrate.

[0002]

[Description of the Related Art]

In a thin film transistor type display device provided with thin film transistors, wiring lines therebetween, and a supporting substrate, there are many cases where the thin film transistors form a part of the whole display device, and the wiring lines and the supporting substrate form the

remaining part thereof. When a thin film transistor type display device is manufactured, through the same manufacturing processes, after the thin film transistors, the wiring lines, and the supporting substrate are integrated, highly complicated manufacturing processes are required to make highly functional thin film transistors. Thus, the manufacturing cost generally increases. However, highly complicated manufacturing processes are not required to make only the wiring lines and the supporting substrate, and the manufacturing cost thereof is low. If the thin film transistors can be made independently from wiring lines or supporting substrate and then disposed only in desired portions, it is possible to lower the manufacturing cost of the thin film transistor type display device if averaged as a whole.

[0003]

Therefore, thin film transistor type display devices have been developed wherein thin film transistors are formed on a first substrate, wiring lines are formed on a second substrate, and an element chip including one or more thin film transistors is peeled off from the first substrate and transferred to the second substrate. According to this method, since the thin film transistors can be disposed only in desired portions, it is possible to lower the manufacturing cost of the thin film transistor type display

device if averaged as a whole. In addition, at this time, laser ablation or adhesive are used as the peeling or transferring process.

[0004]

Fig. 1 is a process view of a method for peeling and transferring an element chip. A peeling layer 12 is formed on a first substrate 11, thin film transistors 13 and connecting pads 14 are formed on the peeling layer 12, and an element chip 16, which is separated with separations 15, is formed. Wiring lines 18 and connecting pads 19 are formed on the second substrate 17, and they are coated with adhesive 1a. The first substrate 11 and the second substrate 17 are pressure-bonded, and the adhesive 1a is caused to flow, thereby electrically connecting the connecting pads 14 of the element chip 16 to the connecting pads 19 of the second substrate 17. The adhesive 1a does not flow to other adjacent element chips 16 due to the separations 15. The element chip 16, including one or more thin film transistors 13, is peeled off from the first substrate 11 by laser ablation with irradiation of a laser 1b, and is transferred to the second substrate 17.

[0005]

Fig. 2 is a plan view of a conventional element chip. An element chip 26 including one or more thin film transistors 25 is formed by using a polycrystalline silicon

layer 21, a first metal layer 22, a second metal layer 23, and contact holes 24. Here, in the patterning processes of all the layers, normal stepper exposure is used, and a design rule with a line/space/alignment precision = 5 μm/5 μm/5 μm is used. The thin film transistors 25 form a pixel circuit of organic light emitting diodes in the element chip 26. The reason why two metal layers such as the first metal layer 22 and the second metal layer 23 are used is that the present thin film transistor type display device requires transverse and longitudinal bus lines in order to display two-dimensional images, and the bus lines should have low resistance to reduce the time constant and voltage drop therein in consideration of the actual size of the thin film transistor type display device. The area of the element chip 26 is 150 μm × 85 μm = 12750 μm^2.

[0006]

Fig. 3 is a process view of a method of manufacturing a conventional element chip. A peeling layer 32 is formed on a first substrate 31, and a base insulating film 33 is formed on the peeling layer 32. An amorphous silicon (a-Si) layer 34 is deposited using PECVD of SiH_4, LPCVD of Si_2H_6, etc., and it is crystallized and patterned with laser irradiation 35 to obtain a polycrystalline silicon (poly-Si) layer 36. A gate insulating film 37 is deposited using PECVD or ECR-CVD of TEOS, etc., a resistive mask 39 is used

to selectively implant dopant ions by ion implantation or ion doping 38, and source/drain regions 3a are formed. Gate metal is deposited and patterned to obtain gate electrodes 3b. The gate electrodes 3b are used to selectively implant dopant ions by ion implantation, ion doping 3c, etc., to form lightly doped drain regions (LDD) 3d. An interlayer insulating film 3e is deposited, and contact holes 3f are formed. Source/drain metal is deposited and patterned to obtain source/drain electrodes 3g. The source/drain electrodes 3g are also used as connecting pads. Thin film transistors 3h are obtained from the above processes. Finally, an element chip 3j is formed by separating with the separations 3i. Although only one element chip 3j is illustrated in Fig. 3, a plurality of element chips 3j is arranged.

[0007]

On the other hand, methods of manufacturing thin film transistors known as holographic exposure or tracking focus (white light focus: WLF) systems have been developed. According to the holographic exposure method, in the patterning process of thin film transistors, a fine design rule, for example, 1.0 μm or less can be used. Further, according to the tracking focus system, since the surface swelling of a large substrate can be compensated for, the exposure can be made with uniformity and high precision.

(For example, refer to the non-patent documents)

[Non-patent Documents]

T. Shimoda, et al, Tech. Dig. IEDM 1999, 289; S. Utsunomiya, et al, Dig. Tech. Pap. SID 2000, 916; T. Shimoda, Proc. Asia Display/IDW '01, 327; S. Utsunomiya, et al, Proc. Asia Display/IDW '01, 339; T. Shimoda, Dig. Tech. Pap. AM-LCD 02, 5; http://www.holtronic.ch.

[0008]

[Problems to be Solved by the Invention]

In the thin film transistor type display device in which thin film transistors are formed on a first substrate, wiring lines are formed on a second substrate, and an element chip including one or more thin film transistors is peeled off from the first substrate and transferred to the second substrate, since the thin film transistors can be disposed only in desired portions, the manufacturing cost of the thin film transistor type display device can be lowered if averaged as a whole. At this time, the size of the element chip affects the manufacturing cost greatly. Therefore, an object of the present invention is to reduce the size of an element chip and lower the manufacturing cost.

[0009]

[Means for Solving the Problems]

In order to solve the above problems, the present invention provides a thin film transistor type display

device in which thin film transistors are formed on a first substrate, wiring lines are formed on a second substrate, and an element chip including one or more thin film transistors is peeled off from the first substrate and transferred to the second substrate, wherein holographic exposure is used in the patterning process of the thin film transistors.

[0010]

According to this configuration, it is possible to use a fine design rule in the patterning process of thin film transistors, reduce the size of element chips, and lower the manufacturing cost.

[0011]

Further, the present invention provides a thin film transistor type display device in which thin film transistors are formed on a first substrate, wiring lines are formed on a second substrate, and an element chip including one or more thin film transistors is peeled off from the first substrate and transferred to the second substrate, wherein a tracking focus system is used in the patterning process of the thin film transistors.

[0012]

According to this configuration, since it is possible to compensate for the surface swelling of a large substrate, it is possible to expose the substrate with high precision

and uniformity, to reduce the size of element chips, and to lower the manufacturing cost.

[0013]

Moreover, the present invention provides the above-mentioned thin film transistor type display device in which a design rule of 1.0 μm or less is used in the patterning process of the thin film transistors.

[0014]

According to this means, exposure can be made with uniformity and high precision using a design rule of 1.0 μm or less by holographic exposure or a tracking focus system, and it is possible to reduce the size of element chips and lower the manufacturing cost.

[0015]

Furthermore, the present invention provides the above-mentioned thin film transistor type display device in which only a polycrystalline silicon layer and a first metal layer are used as the wiring lines of the element chip.

[0016]

According to the this configuration, it is possible to further lower the manufacturing cost by simplifying the manufacturing processes while keeping the size-reduction effect of element chips in the holographic exposure or tracking focus system.

[0017]

Further, in order to solve the above problems, the present invention provides a method of manufacturing thin film elements including a step of transferring functional elements formed on a first substrate to a second substrate, the method comprising the steps of: forming the functional elements in a predetermined shape on the first substrate via a peeling layer which causes peeling by the application of a predetermined amount of energy, and transferring at least one of the functional elements to the second substrate by applying the energy to relevant portions of the peeling layer corresponding to the regions of the functional elements to cause peeling, wherein holographic exposure is used to pattern the functional elements in the step of forming the functional elements in a predetermined shape.

[0018]

Further, the functional elements are preferably thin film transistors.

[0019]

Further, the present invention provides a thin film transistor circuit board, an electro-optical device, and an electronic apparatus which comprise the above thin film transistors.

[0020]

[Description of the Embodiments]

Hereinafter, preferred embodiments of the present

invention will be explained. In addition, a series of aspects about a transfer method is also described in Japanese Patent Application Nos. 2001-282423, 2001-282424, etc., which are disclosed by the present applicant.

[0021]

Fig. 4 is a plan view of an element chip according to an embodiment of the present invention. An element chip 45 including one or more thin film transistors 44 is formed by using a polycrystalline silicon layer 41, a first metal layer 42, and contact holes 43. Here, in the patterning processes of the polycrystalline silicon layer 41 and the first metal layer 42, holographic exposure or a tracking focus system is used, and a design rule of line/space = 1 μm/1 μm is used. In the patterning processes of other layers, normal stepper exposure is used, and a design rule of line/space = 5 μm/5 μm is used. In the patterning processes of all the layers, a design rule with an alignment precision = 5 μm is used. The thin film transistors 44 form a pixel circuit of organic light emitting diodes in the pixel chip 45. Although only the polycrystalline silicon layer 41 and the first metal layer 42 are used, the time constant and voltage drop do not cause problems because the element chip 45 is small compared to the overall size of the display device. The area of the element chip 45 is 115 μm × 69 μm = 7935 μm^2, which is reduced to 62% compared to a

conventional element chip.

[0022]

Fig. 5 is a process view of a method of manufacturing an element chip according to an embodiment of the present invention. A peeling layer 52 is formed on a first substrate 51, and a base insulating film 53 is formed on the peeling layer 52. An amorphous silicon (a-Si) layer 54 is deposited using PECVD of SiH_4 or LPCVD of Si_2H_6, etc. is crystallized and patterned with laser irradiation 55 so as to obtain a polycrystalline silicon (poly-Si) layer 56. A gate insulating film 57 is deposited using PECVD, ECR-CVD, etc., of TEOS, a resistive mask 59 is used to selectively implant dopant ions by ion implantation or ion doping 58, source/drain regions 5a are formed, and contact holes 5b are formed. Gate metal is deposited and patterned to obtain gate electrodes 5c. The gate electrodes 5c are also used as source/drain electrodes or connecting pads. The gate electrodes 5c are used to selectively implant dopant ions by ion implantation, ion doping, 5d etc., to form lightly doped drain regions (LDD) 5e. Thin film transistors 5f are obtained from the above processes. Finally, element chips 5h are formed by separating with separations 5g. In Fig. 5, only one element chip 5h is illustrated. However, a plurality of element chips 5h is actually arranged.

[0023]

In the present embodiment, as described in Claim 1, in the patterning process of the thin film transistors 44, holographic exposure is used. Further, as defined in Claim 2, in the patterning process of the thin film transistors 44, a tracking focus system is used. Further, as described in Claim 3, in the patterning process of the thin film transistors 44, a design rule of 1.0 μm or less is used. Further, only the polycrystalline crystal silicon layer 41 and the first metal layer 42 are used as wiring lines of the element chip 45.

[0024]

Moreover, in the present embodiment, in the patterning processes of the polycrystalline silicon layer 41 and the first metal layer 42, holographic exposure and a tracking focus system are used, and a design rule of line/space = 1 μm/1 μm is used. However, even though the holographic exposure and the tracking focus system are used in the patterning processes of other layers and then the design rule of line/space = 1 μm/1 μm is used, the idea of the present invention applies.

[0025]

Further, the present invention can be applied to a liquid crystal electro-optical device which uses an active matrix substrate. The active matrix substrate of each of the above-mentioned embodiments to which the present

invention is applied can lower cost and improve quality compared with an electro-optical device, which is manufactured using a conventional active matrix substrate. Of course, although the liquid crystal electro-optical device is illustrated as the electro-optical device, the present invention can also be applied to other electro-optical devices such as organic electroluminescent device and electrophoresis display devices.

[0026]

Further, since these electro-optical devices are mounted on electronic apparatuses, for example, portable telephones, etc., the present invention can provide electronic apparatuses to enjoy the above advantages.

[Brief Description of the Drawings]

[Fig. 1]

Fig. 1 is a process view of a method for peeling and transferring an element chip.

[Fig. 2]

Fig. 2 is a plan view of a conventional element chip.

[Fig. 3]

Fig. 3 is a process view of a method of manufacturing a conventional element chip.

[Fig. 4]

Fig. 4 is a plan view of an element chip according to an embodiment of the present invention.

[Fig. 5]

Fig. 5 is a process view of a method of manufacturing an element chip according to an embodiment of the present invention.

[Reference Numerals]

11: FIRST SUBSTRATE

12: PEELING LAYER

13: THIN FILM TRANSISTOR

14: ELEMENT CHIP CONNECTING PAD

15: SEPARATION

16: ELEMENT CHIP

17: SECOND SUBSTRATE

18: WIRING LINE

19: CONNECTING PAD OF SECOND SUBSTRATE

1a: ADHESIVE

1b: LASER

21: POLYCRYSTALLINE SILICON LAYER

22: FIRST METAL LAYER

23: SECOND METAL LAYER

24: CONTACT HOLE

25: THIN FILM TRANSISTOR

26: ELEMENT CHIP

31: FIRST SUBSTRATE

32: PEELING LAYER

33: BASE INSULATING FILM

34: AMORPHOUS SILICON (a-Si) LAYER

35: LASER IRRADIATION

36: POLYCRYSTALLINE SILICON (poly-Si) LAYER

37: GATE INSULATING FILM

38: ION IMPLANTATION OR ION DOPING

39: RESIST MASK

3a: SOURCE/DRAIN REGION

3b: GATE ELECTRODE

3c: ION IMPLANTATION OR ION DOPING

3d: LIGHTLY DOPED DRAIN REGION (LDD)

3e: INTERLAYER INSULATING FILM

3f: CONTACT HOLE

3g: SOURCE/DRAIN ELECTRODE

3h: THIN FILM TRANSISTOR

3i: SEPARATION

3j: ELEMENT CHIP

41: POLYCRYSTALLINE SILICON LAYER

42: FIRST METAL LAYER

43: CONTACT HOLE

44: THIN FILM TRANSISTOR

45: ELEMENT CHIP

51: FIRST SUBSTRATE

52: PEELING LAYER

53: BASE INSULATING FILM

54: AMORPHOUS SILICON (a-Si) LAYER

55: LASER IRRADIATION

56: POLYCRYSTALLINE SILICON (poly-Si) LAYER

57: GATE INSULATING FILM

58: ION IMPLANTATION OR ION DOPING

59: RESIST MASK

5a: SOURCE/DRAIN REGION

5b: CONTACT HOLE

5c: GATE ELECTRODE

5d: ION IMPLANTATION OR ION DOPING

5e: LIGHTLY DOPED DRAIN REGION (LDD)

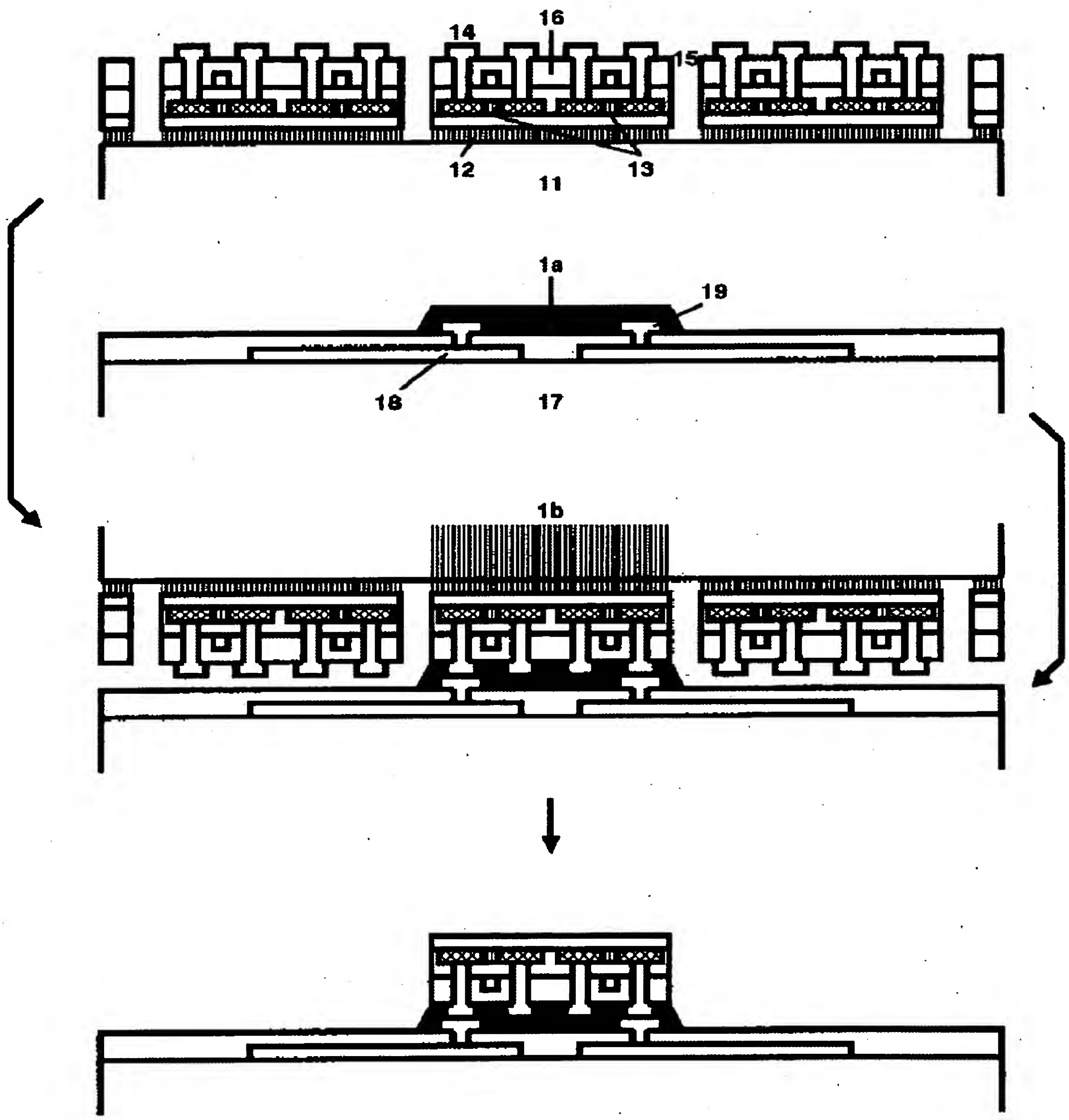
5f: THIN FILM TRANSISTOR

5g: SEPARATION

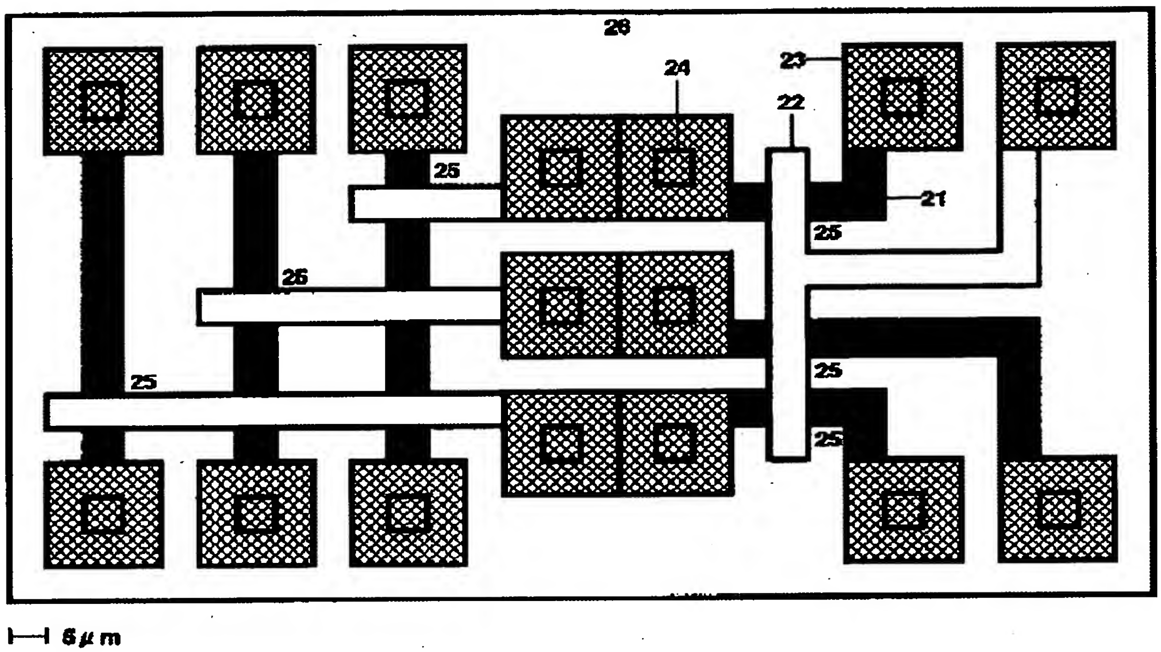
5h: ELEMENT CHIP

[Name of Document] DRAWINGS

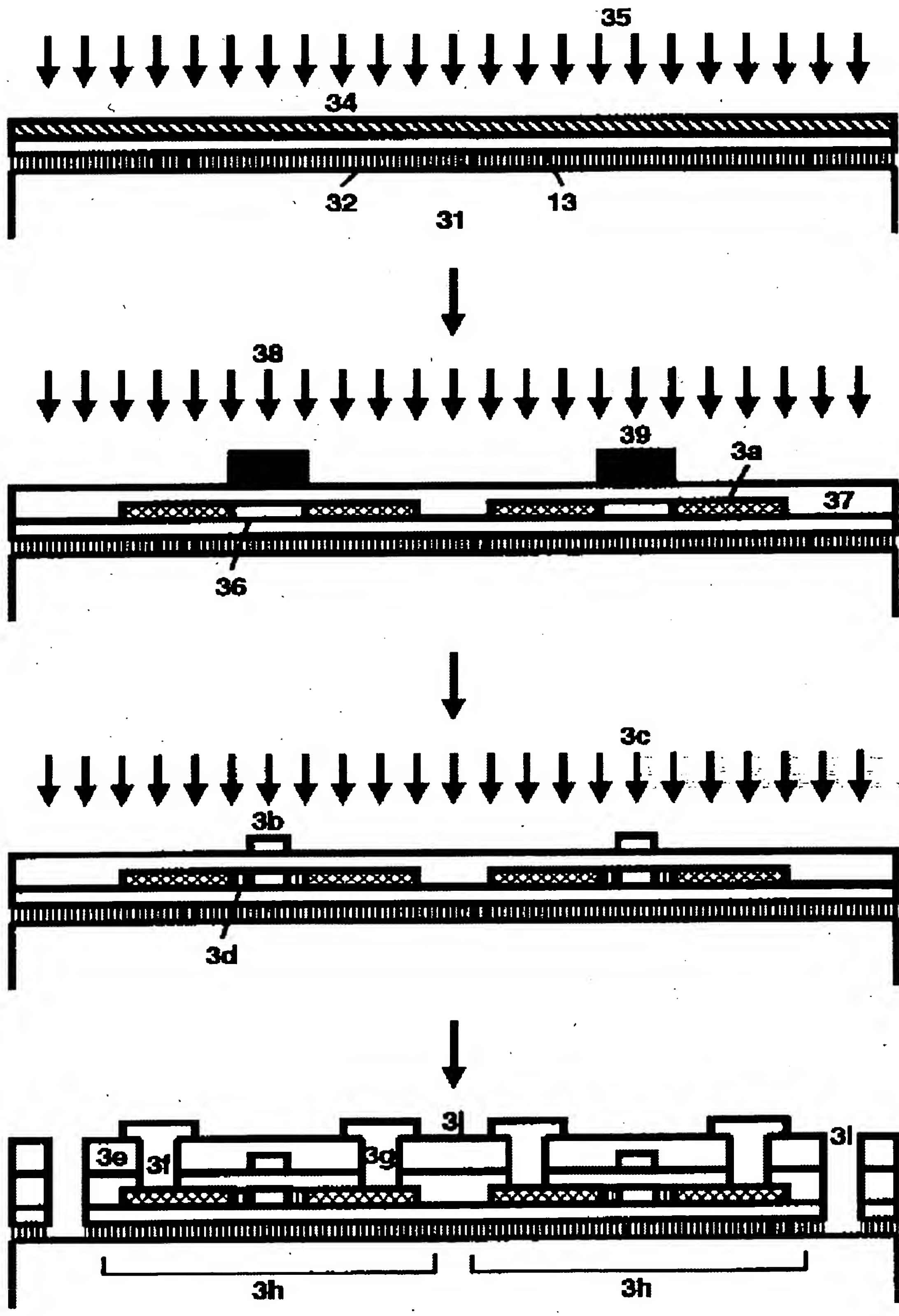
[FIG. 1]



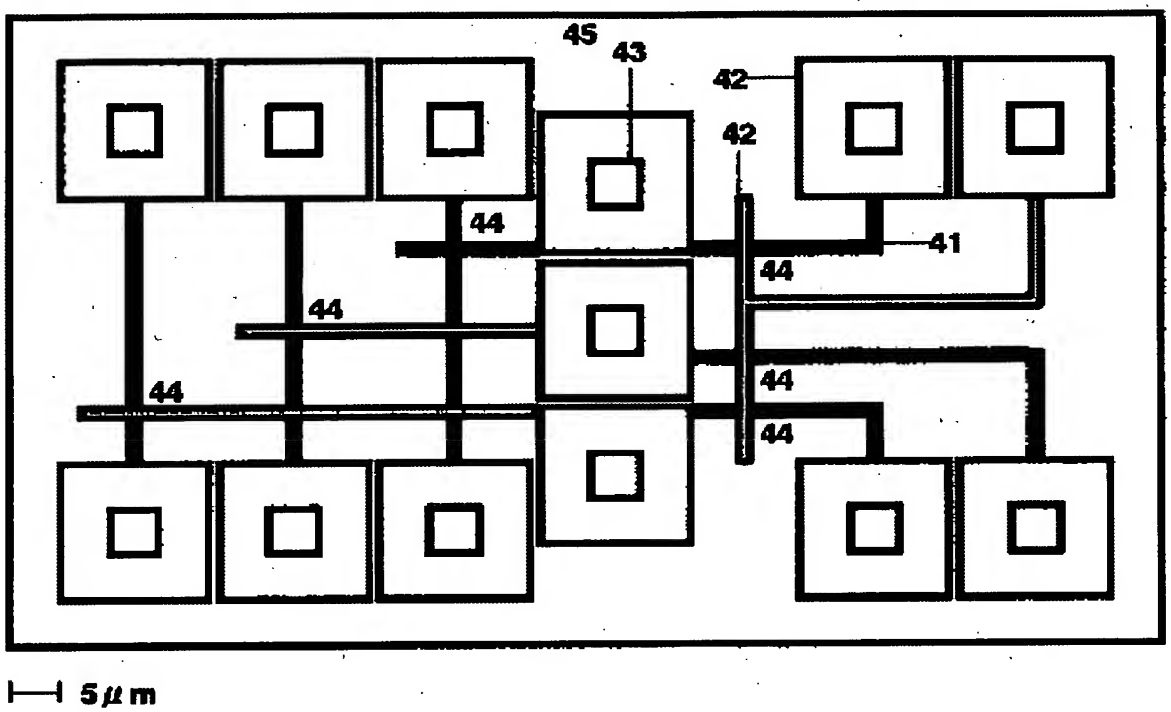
[FIG. 2]



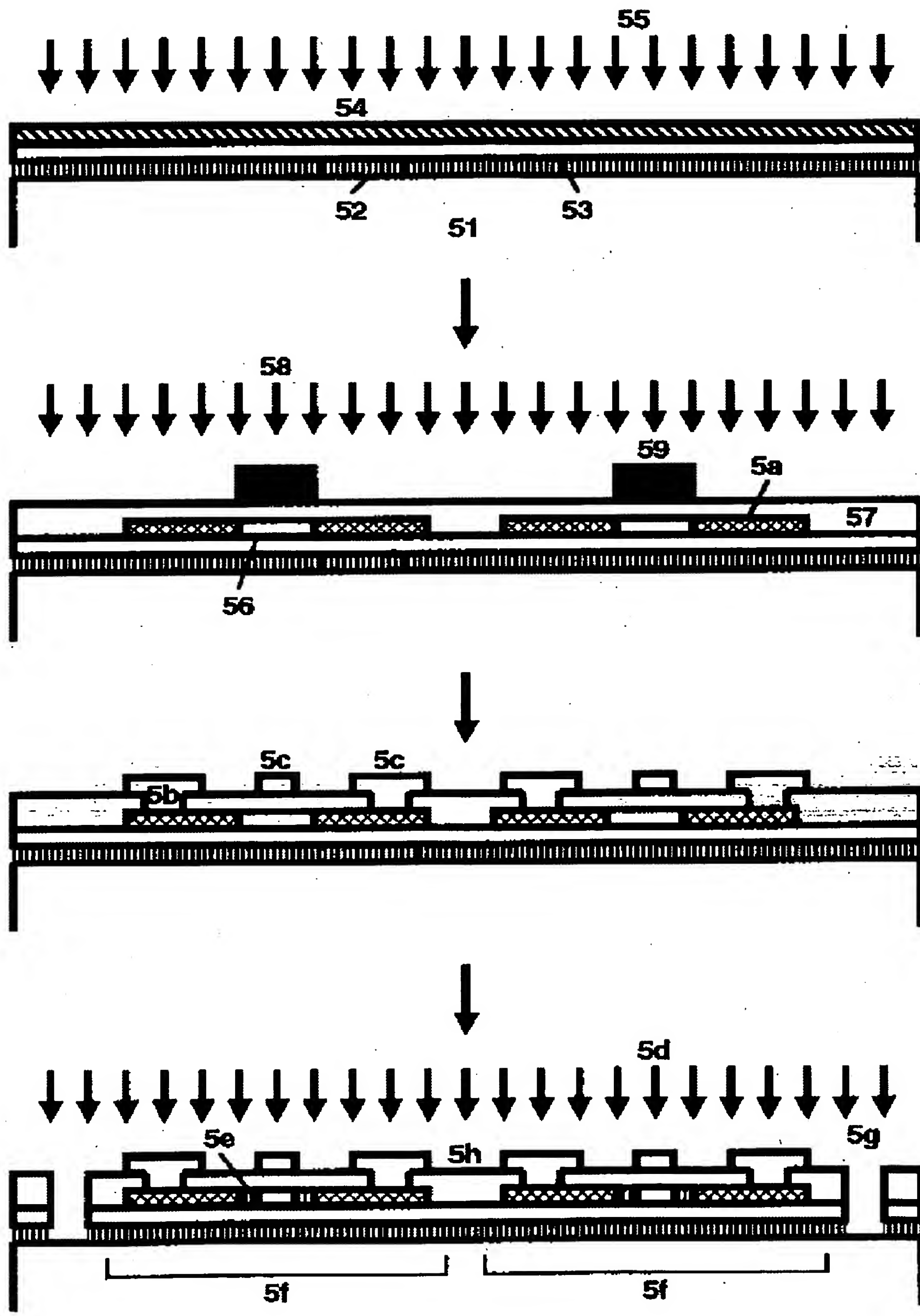
[FIG. 3]



[FIG. 4]



[FIG. 5]



[Name of Document] ABSTRACT

[Abstract]

[Object] To reduce the size of an element chip 45 and lower the manufacturing cost in a thin film transistor type display device in which thin film transistors 44 are formed on a first substrate, wiring lines are formed on a second substrate, and the element chip 45, including one or more thin film transistors 44, is peeled off from the first substrate and transferred to the second substrate.

[Solving Means] In the patterning process of the thin film transistors 44, holographic exposure or a tracking focus system is used, a design rule of 1.0 μm or less is used, and only a polycrystalline silicon layer 41 and a first metal layer 42 are used as the wiring lines of the element chip 45.

[Selected Figure] Fig. 4